ABSTRACT OF THE DISCLOSURE

Electroless plating can be utilized to form electrical interconnects associated with semiconductor substrates. For instance, a semiconductor substrate can be formed to have a dummy structure thereover with a surface suitable for electroless plating, and to also have a digit line thereover having about the same height as the dummy structure. A layer can be formed over the dummy structure and digit line, and openings can be formed through the layer to the upper surfaces of the dummy structure and digit line. Subsequently, a conductive material can be electroless plated within the openings to form electrical contacts within the openings. The opening extending to the dummy structure can pass through a capacitor electrode, and accordingly the conductive material formed within such opening can be utilized to form electrical contact to the capacitor electrode.